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Generalized space vector controls for MLZSI

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KEYWORDS

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THD

Abstract This paper proposes two advanced algorithms for multilevel Z-source inverter (MLZSI), which employ space vector control (SVC) as control algorithm of cascaded H-bridge multilevel Z-source inverter; where output voltage is achieved by summing the output voltages of bridge. In these algorithms different states to generate the same voltage with low THD, as the purpose, are verified and the suitable one is selected. This method is simple and has appropriate performance, where sample time is set quietly. Use of Z-network allows the inverter to generate a wide range of output voltage with high reliability. The accuracy of suggested algorithms is validated with simulation results using MATLAB/SIMULINK software and experimental results based PCI-1716 data acquisition system.

1. Introduction

Power inverters of both two-level and multilevel configurations have so far been broadly applied to a vast number of dc–ac power inversion applications, including ac motor drives, renewable energy interfacing and uninterruptable power supplies [1–6].

The modulation methods used in multilevel inverters can be classified according to switching frequency [6–9]. SVC first proposed in [7]. This control strategy works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of SVM [6]. This method, also, produces a high-quality load voltage working [1]. In addition, SVC, in general, has better performance than carrier-based PWM methods. The vector control strategy is simple and it can be easily implemented in a standard DSP motor controller [1].

A very attractive alternative in multilevel energy conversion is the cascaded topology which uses the series connection of multiple single-phase voltage-source inverters (VSIs) [4] where the output phase voltage waveform of a cascaded inverter with isolated dc voltage sources is achieved by summing the output voltages of bridges. Total harmonic distortion (THD) is used for the evaluation in multilevel inverter. THD is defined as follows:

$$\%\mathrm{THD} = 100\sqrt{\sum_{k\neq 1}\left(\frac{V_k}{V_1}\right)^2} \quad (1)$$

where k is the number of harmonics.

For the boost or buck of multilevel output voltage a DC/DC converter is needed. Z-source converter (ZSC) a novel power converter with both buck and boost capabilities was first proposed in 2002 [10]. The benefits of the Z-source

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Nomenclature

V_{dc}	dc voltage	v_{AN}, v_{BN} and v_{CN}	voltages of terminals A, B and C
v_i	output voltage of impedance network	a	complex operator
B	boost factor	v_x and v_y	components of voltage in x and y axes
T	period of switching	v_{ref}	reference voltage
T_{st}	total shoot-through state period	v_{pu}	per unit voltage
V_{SC}	straight line for control of shoot-through state in PWM	v_{des}	desired fundamental voltage
		m_a	modulation index
V_{ca}	peak value of triangle waveform in PWM	n	shoot-through states
T_{ca}	triangle period time in PWM	L	number of shoot-through state of n
T_1	shoot-through time during quarter of triangle period time in PWM	S	sample accuracy of m_a

inverter (ZSI) are lower costs, lower complexity, higher reliability and higher efficiency compared to traditional inverters [11]. Most recent publications have focused on modified pulse width modulation (PWM) switching algorithms for Z-source inverter [10,12]. In order to produce flexible ac output voltage, a modified PWM strategy must be applied with proper shoot-through duty ratio [10,13].

This paper proposes the development of Z-source inverter based on SVC algorithm. It also suggests two advanced SVC algorithms for multilevel Z-source inverter. Cascaded H-bridge topology is used as a multilevel inverter combined with Z-source inverter. Sections 2 and 3 present the working principle of the advanced algorithms. For verifying these strategies, simulations are performed with their captured results presented in Section 4.

2. Cascaded H-bridge multilevel Z-source inverter

The Z-source inverter structure is shown in Fig. 1. With the analyses of circuit, v_i is obtained as [10,14]:

$$v_i = \left(\frac{1}{1-2\frac{T_{st}}{T}}\right) V_{dc} \tag{2}$$

$$B = \frac{1}{1-2\frac{T_{st}}{T}} \tag{3}$$

Fig. 2 shows the cascaded H-bridge 5-level Z-source inverter. The output voltage is achieved by summing the output voltages of bridge. Each H-bridge inverter can generate three different voltage outputs $+v_i$, 0, $-v_i$ [2].

This configuration, unlike the traditional multilevel inverters, has one extra zero state (or vector) when the terminals of each H-bridge are shorted through both the upper and lower devices of any one leg or any two legs. So each H-bridge is turned into shoot-through state when the output voltage level is traditional zero.

Table 1 indicates the values of v_o for possible states of switches in cascaded H-bridge 5-level Z-source inverter.

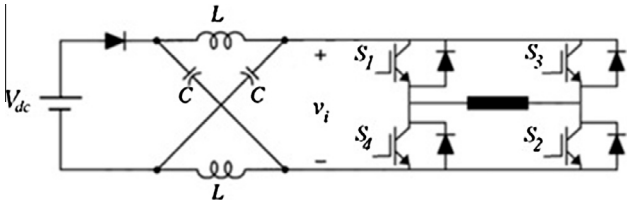


Figure 1 Z-source inverter structure.

3. Switching algorithms

3.1. PWM

The most common algorithm among switching methods is the sinusoidal pulse width modulation (SPWM). This algorithm is based on a comparison of a sinusoidal reference waveform and carrier triangular waveforms. Each H-bridge uses two triangular waveforms for PWM switching, and one straight line (V_{SC}) to control of shoot-through state time. When carrier waveform is greater than V_{SC} or lower than $-V_{SC}$, the related H-bridge turns into shoot-through state and otherwise the inverter operates just as traditional PWM. So, boost factor of this inverter can be controlled by the value of V_{SC}. Fig. 3 shows waveforms for shoot-through state. Then it can be obtained as follows:

$$\frac{T_{st}}{T} = \frac{T_1}{\frac{T_{ca}}{4}} \tag{4}$$

where T_1 is shoot-through time during half of triangles period time, T_{ca}. It is clear that:

$$\frac{T_1}{\frac{T_{ca}}{4}} = \frac{V_{ca}-V_{SC}}{V_{ca}} \tag{5}$$

Therefore, boost factor is obtained as follows:

$$B = \frac{1}{1-2\left(\frac{V_{ca}-V_{SC}}{V_{ca}}\right)} \tag{6}$$

3.2. Advanced SVC algorithms

This control method is based on the voltage vector generated by the inverter, defined as [1]:

$$v(t) = \frac{2}{3}\left[v_{AN}(t) + a v_{BN}(t) + a^2 v_{CN}(t)\right] \tag{7}$$

where v_{AN}, v_{BN} and v_{CN} are the voltages of terminals A, B and C with respect to the neutral N. Considering the cascaded H-

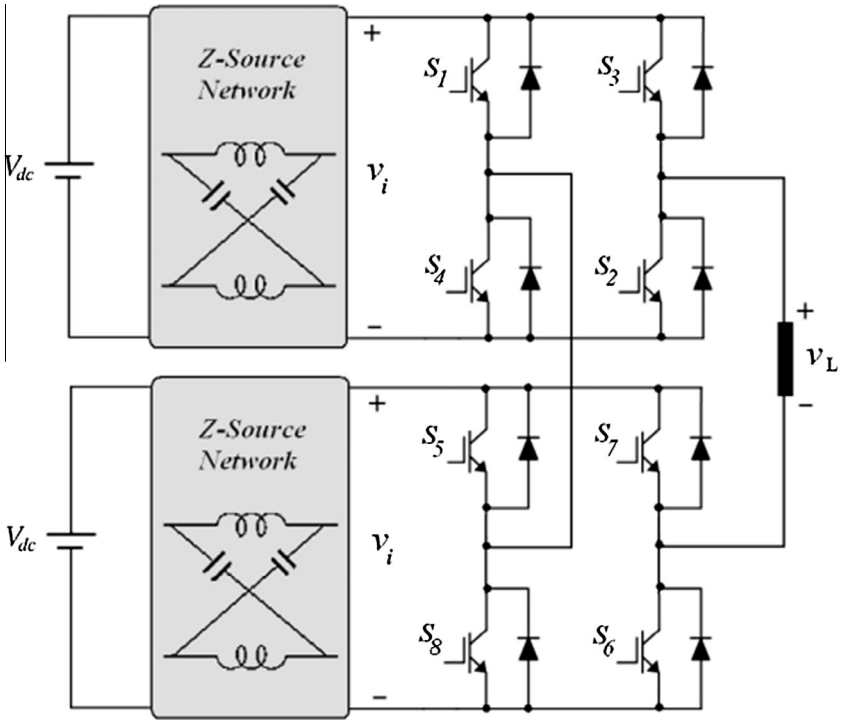


Figure 2 Configuration of the cascaded H-bridge 5-level Z-source inverter.

Table 1 Possible states of switches.

Voltage level	Output voltage	ON switches
Level 2 (non shoot-through)	$2V_{in}$	S_3, S_4, S_5, S_6
Level 1 (non shoot-through)	V_{in}	S_1, S_3, S_5, S_6
Level 1 (shoot-through)	V_{in}	S_1, S_2, S_3, S_4, S_5, S_6
Level 1 (non shoot-through)	V_{in}	S_3, S_4, S_5, S_7
Level 1 (shoot-through)	V_{in}	S_3, S_4, S_5, S_6, S_7, S_8
Level 0 (non shoot-through)	0 (V)	S_3, S_4, S_7, S_8
Level 0 (shoot-through)	0 (V)	—
Level 0 (non shoot-through)	0 (V)	S_1, S_3, S_5, S_7
Level 0 (shoot-through)	0 (V)	S_1, S_2, S_3, S_4, S_5, S_7
Level 0 (shoot-through)	0 (V)	S_1, S_3, S_5, S_6, S_7, S_8
Level −1 (non shoot-through)	$-V_{in}$	S_1, S_3, S_7, S_8
Level −1 (shoot-through)	$-V_{in}$	S_1, S_2, S_3, S_4, S_7, S_8
Level −1 (non shoot-through)	$-V_{in}$	S_1, S_2, S_5, S_7
Level −1 (shoot-through)	$-V_{in}$	S_1, S_2, S_5, S_6, S_7, S_8
Level −2 (non shoot-through)	$-2V_{in}$	S_1, S_2, S_7, S_8

bridge 7-level inverter with 3 cells per phase, each phase can generate 7 different voltages. The representation of the voltage vectors in the complex plane considers that [1]:

$$v(t) = v_x + jv_y \tag{8}$$

where v_x and v_y correspond to the components of $v(t)$ in the x and y axes, respectively. These components are given by [1]:

$$v_x = \frac{1}{3}(2v_{AN} - v_{BN} - v_{CN}) \tag{9}$$

$$v_y = \frac{1}{\sqrt{3}}(v_{BN} - v_{CN}) \tag{10}$$

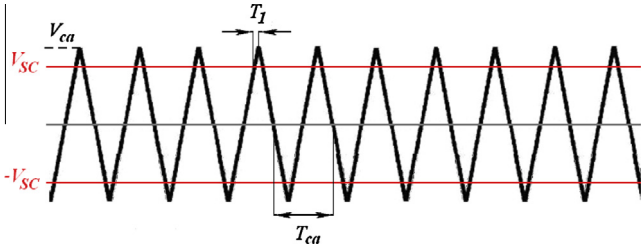


Figure 3 Modulation waveforms for shoot-through state.

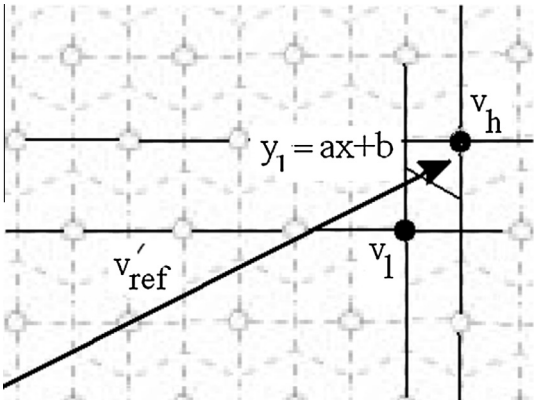


Figure 4 An enlarged representation voltage vector.

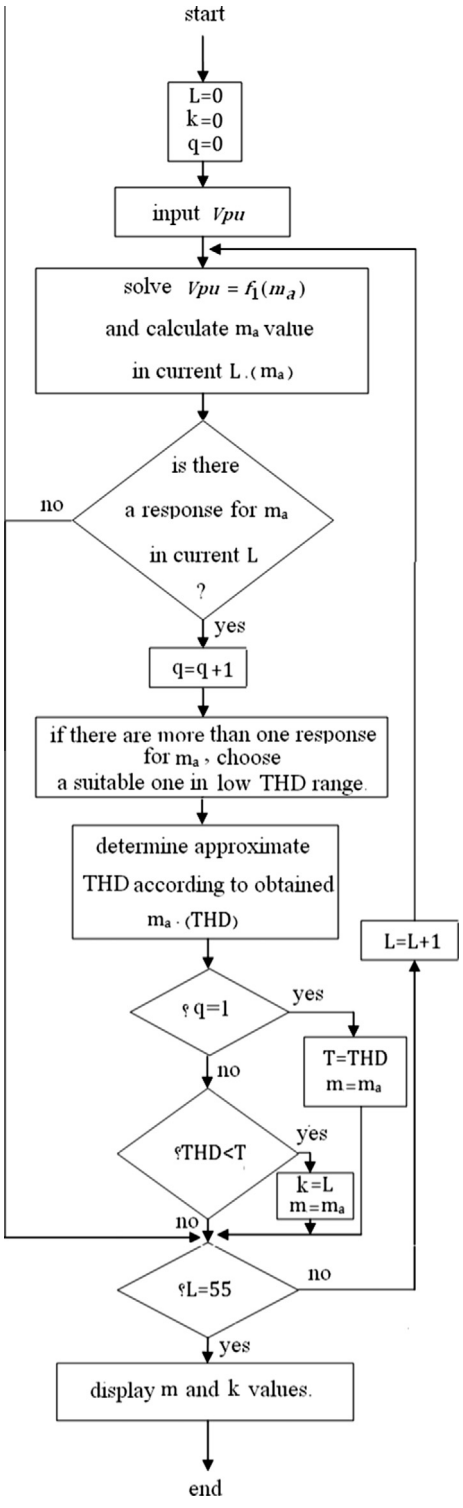


Figure 5 Flowchart of first advanced algorithm for 7-level Z-source inverter.

The main idea of SVC strategy is to select a voltage vector that minimizes the space error according to a reference vector v'_{ref}. Fig. 4 shows an enlarged representation of different vectors generated by the inverter. The control strategy must determine in which hexagon the reference vector is located [1].

The decision between v_h and v_l is done by the following relation [1]:

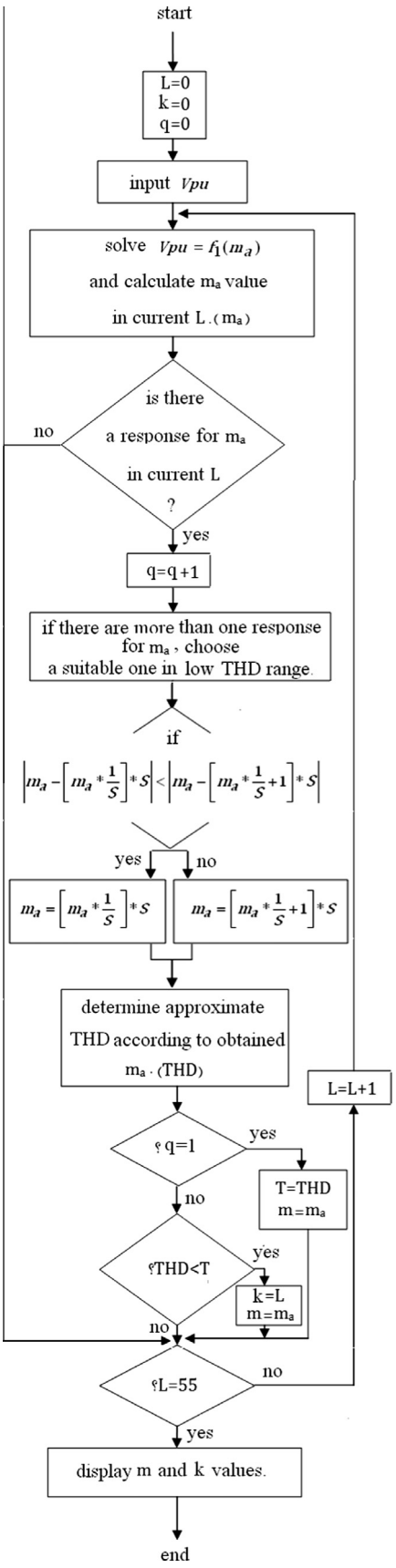


Figure 6 Flowchart of second advanced algorithm for 7-level Z-source inverter.

Table 2 System parameters.

V_{dc}	100 V
$L_1 = L_2$	5 mH
$C_1 = C_2$	2100 μF
Nominal frequency	60 Hz
Load impedance	100 Ω
P.F. of load	1

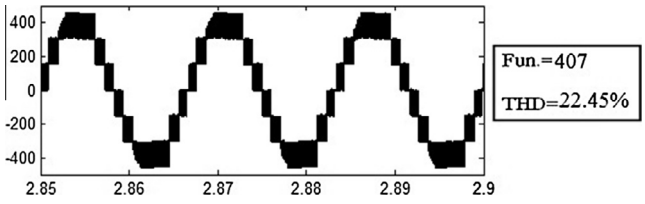


Figure 7 Output voltage of PWM for fundamental = 400 V.

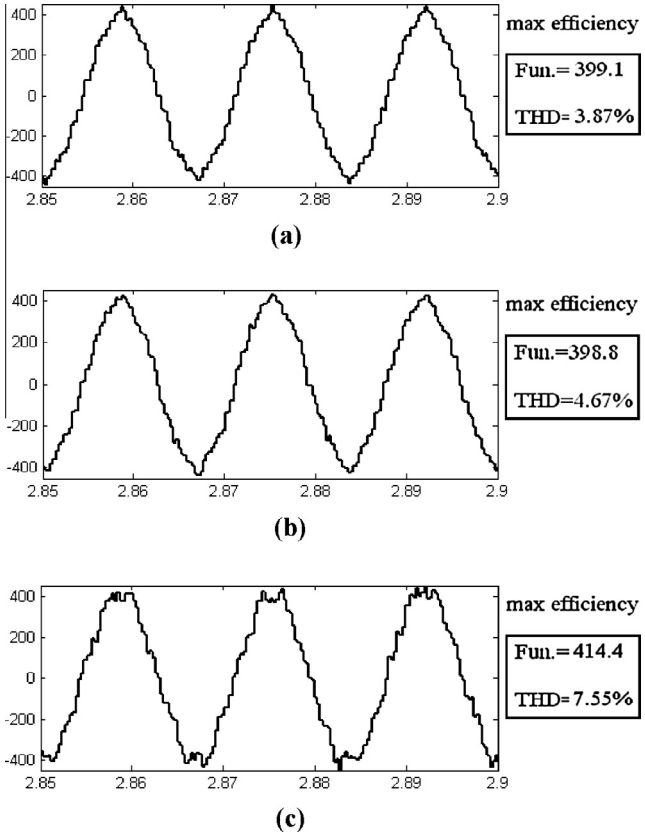


Figure 8 Output voltage of first advanced algorithm for fundamental = 400 V; (a) $n = 5$ and $m_a = 1.063$; (b) $n = 0$, 1 and $m_a = 1.1$; (c) $n = 0$, 2 and $m_a = 0.95$.

$$\text{if } v_y > av_x + b \text{ then } \quad v_{sel} = v_h \qquad \textit{else } v_{sel} = v_l \tag{11}$$

where $v_{sel} = v_{sx} + jv_{sy}$ is the selected vector, delivered by the inverter.

In this algorithm, T_{st} cannot be determined simply. Thus, it should be defined equivalent boost factor (B). Equivalent B is calculated from comparison between lack and presence of Z-network in inverters.

In this section, different states (n) to generate the same output voltage with low THD, as the purpose, are verified. So, the following algorithm is suggested:

$$v_{pu}(m_a, B) = \frac{v_{des}}{V_{dc}} \tag{12}$$

where v_{des} is desired fundamental voltage and m_a is modulation index. Because of dependence of B on m_a, it can be written as follows:

$$v_{pu} = f_1(m_a) = f_2(B) \tag{13}$$

where f_1 and f_2 can be approximated based on numerical data. In this paper, thirteen order approximation is used.

Figs. 5 and 6 show advanced algorithms for the determination of n and m_a. In this flowchart, L is the number of shoot-through state of n, where $0 \leqslant L \leqslant 55$ for 7-level inverter. m and k are m_a and the number of n as response of the algorithms, respectively, and S is sample accuracy of m_a. The difference between these algorithms is appeared when: $m_a * \frac{1}{S} \neq [m_a * \frac{1}{S}]$. In other words, m_a will not be sample modulation index. Thus, in sample modulation indexes, these two algorithms are equal.

Use of these algorithms makes it possible to achieve a wide range of output voltage.

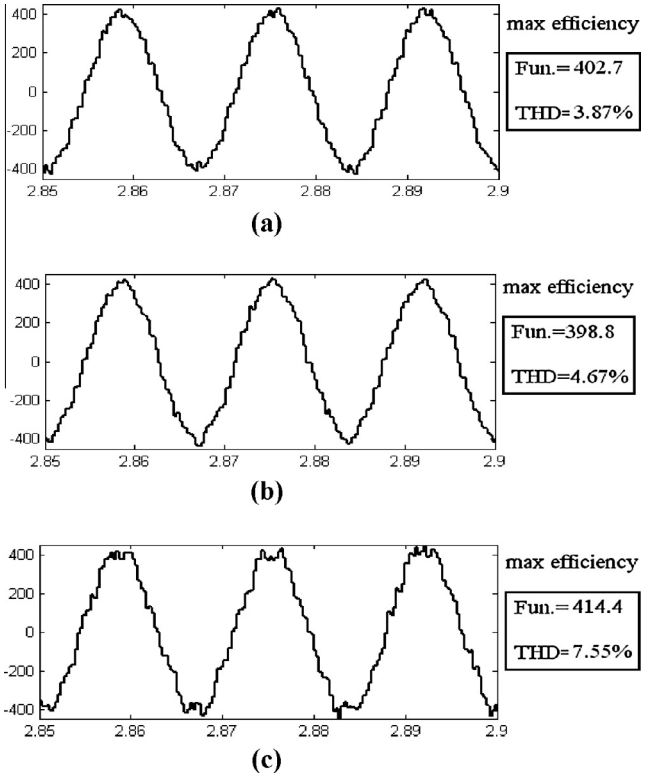


Figure 9 Output voltage of second advanced algorithm for fundamental = 400 V; (a) $n = 5$ and $m_a = 1.05$; (b) $n = 0$, 1 and $m_a = 1.1$; (c) $n = 0$, 2 and $m_a = 0.95$.

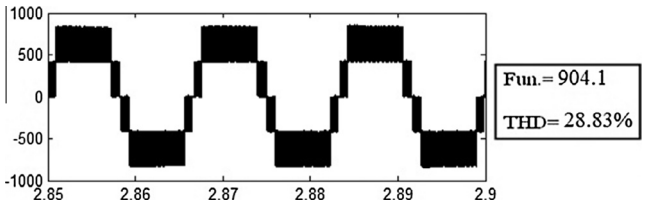


Figure 10 Output voltage of PWM for fundamental = 900 V.

4. Results

4.1. Simulation results

Simulations have been performed to validate the suggested algorithms. In these simulations, cascaded H-bridge 7-level Z-source inverter is employed. The system parameters are listed in Table 2.

In this section, the output voltage is classified into two groups: (a) low voltage, and (b) high voltage.

4.1.1. Low voltage

This group signifies $v_{pu} \leqslant 6$. Figs. 7–9 show output voltages of inverter based on PWM and the suggested algorithm in different n and m_a for (for example) 400 V. It can be observed that THD of PWM is more than suggested algorithms base SVC, significantly. Then, SVC is better choice from viewpoint of THD. The outputs of two suggested algorithms are the same in $n = 0, 1$ and $n = 0, 2$, since m_a is sample modulation index. But in $n = 5$, there is a difference between two algorithms, because: $m_a * \frac{1}{S} \neq [m_a * \frac{1}{S}]$. Although $n = 5$ is the best one because of suitable voltage with low THD that it is choice of two advanced algorithms.

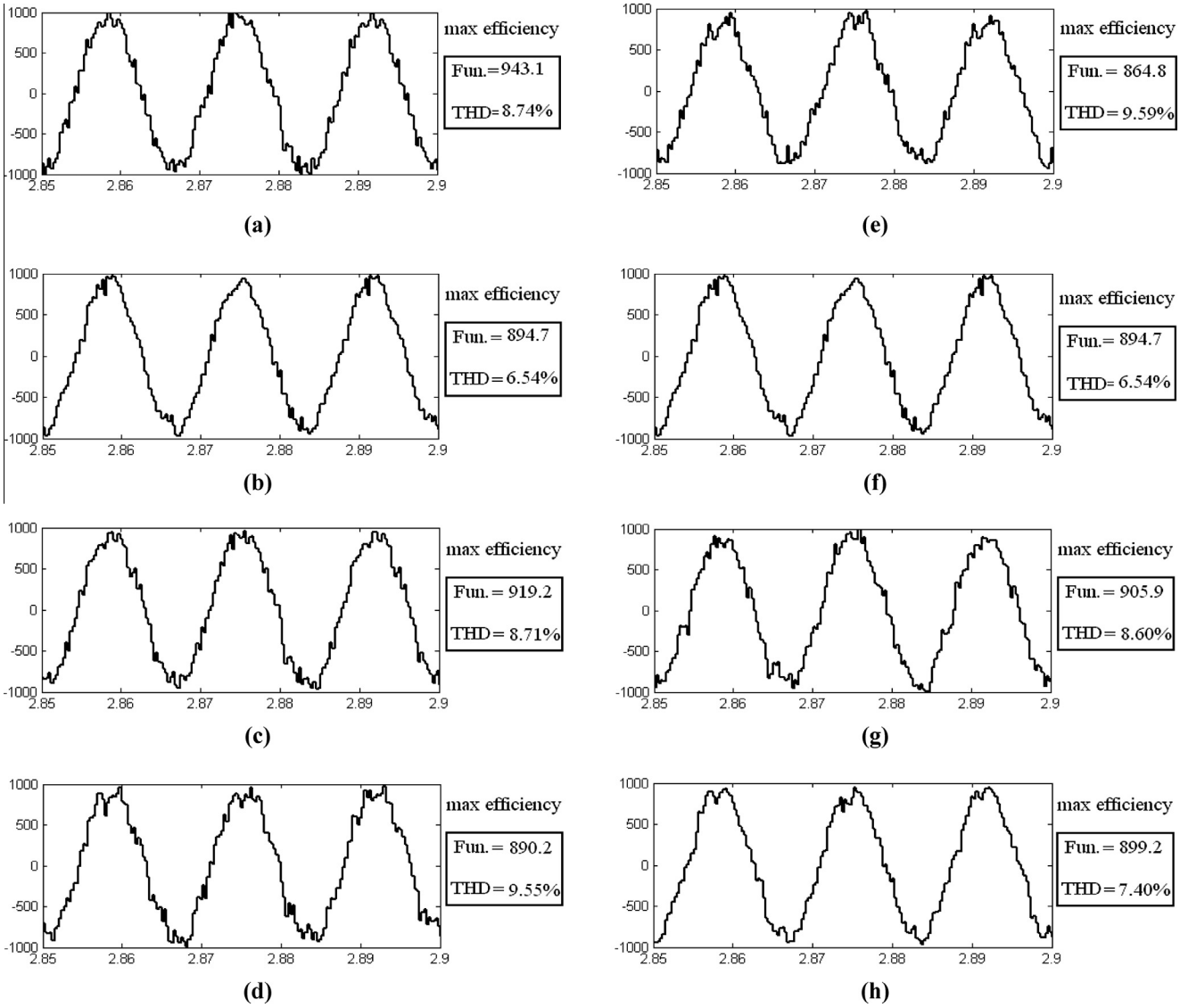


Figure 11 Output voltage of first advanced algorithm for fundamental = 900 V; (a) $n = 1, 2, 3$ and $m_a = 0.957$; (b) $n = 1, 2, 3, 4$ and $m_a = 1.1$; (c) $n = 1, 2, 3, 5$ and $m_a = 0.96$; (d) $n = 1, 2, 4, 5$ and $m_a = 0.945$; (e) $n = 1, 3, 4, 5$ and $m_a = 0.964$; (f) $n = 0, 1, 2, 3, 4$ and $m_a = 1.1$; (g) $n = 0, 1, 2, 3, 5$ and $m_a = 1.023$; (h) $n = 0, 2, 3, 4, 5$ and $m_a = 1.094$.

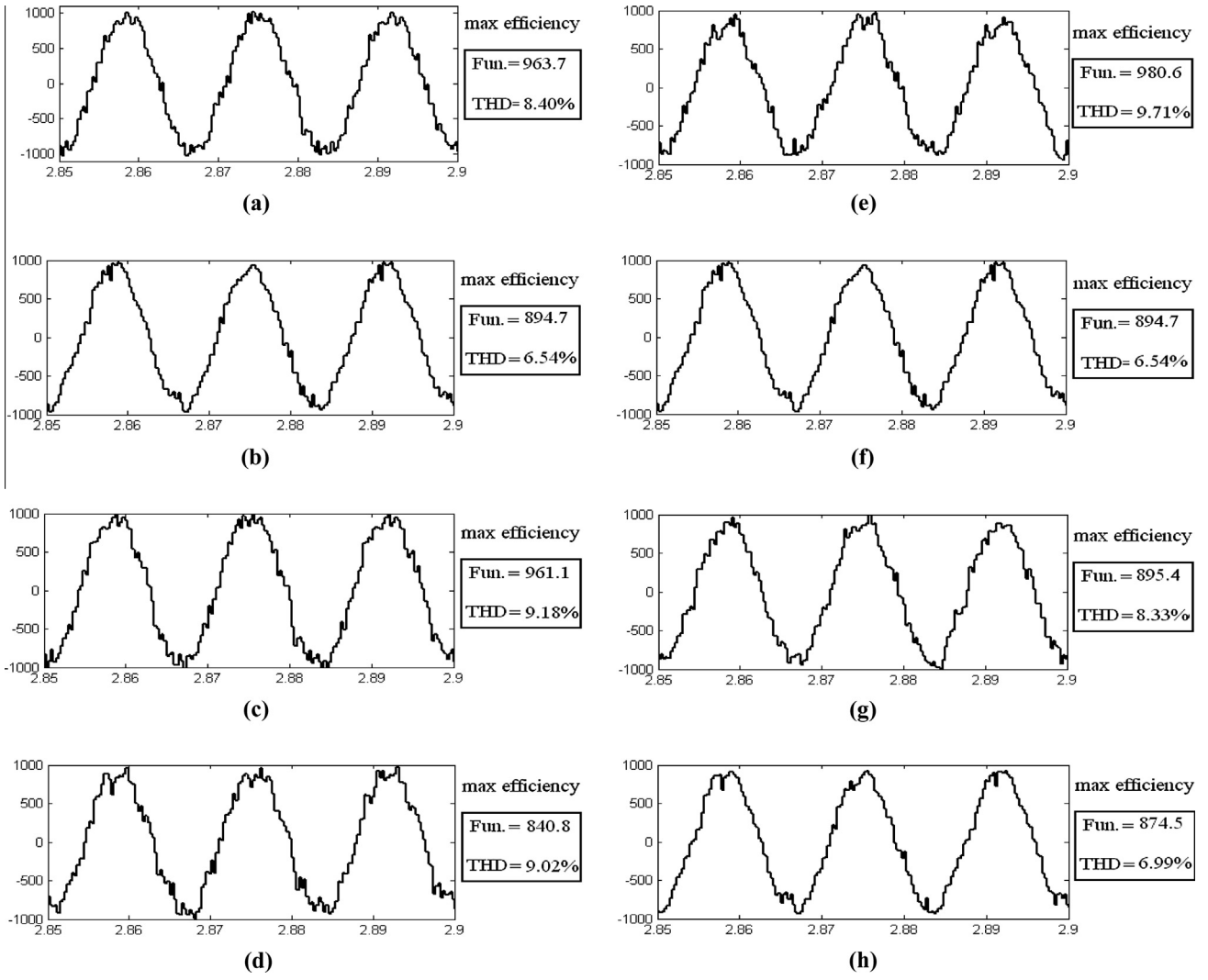


Figure 12 Output voltage of second advanced algorithm for fundamental = 900 V; (a) $n = 1, 2, 3$ and $m_a = 0.95$; (b) $n = 1, 2, 3, 4$ and $m_a = 1.1$; (c) $n = 1, 2, 3, 5$ and $m_a = 0.95$; (d) $n = 1, 2, 4, 5$ and $m_a = 0.95$; (e) $n = 1, 3, 4, 5$ and $m_a = 0.95$; (f) $n = 0, 1, 2, 3, 4$ and $m_a = 1.1$; (g) $n = 0, 1, 2, 3, 5$ and $m_a = 1$; (h) $n = 0, 2, 3, 4, 5$ and $m_a = 1.1$.

4.1.2. High voltage

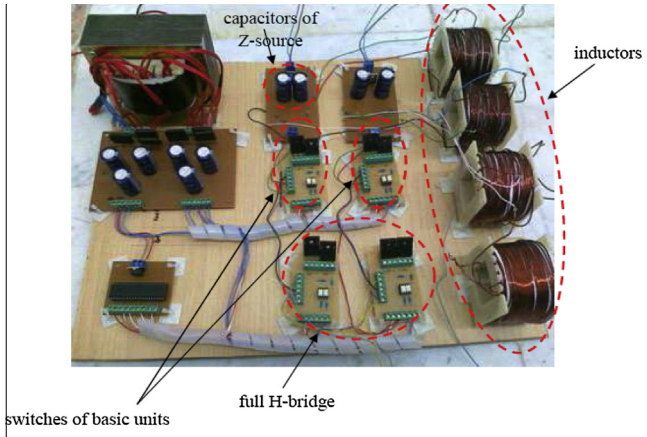
Medium voltage means the range of $6 \leqslant v_{pu}$. In Figs. 10–12, output voltage of inverter for (for example) 900 V is displayed. From this figures it is evident that, for first advanced SVC algorithm, shoot-through implementation in $n = 0, 1, 2, 3, 4$, $n = 1, 2, 3, 4$, and $n = 0, 2, 3, 4, 5$ and for second advanced algorithm shoot-through implementation in $n = 0, 1, 2, 3, 4$, and $n = 1, 2, 3, 4$ have appropriate performance which advanced algorithms select $n = 0, 1, 2, 3, 4$ or $n = 1, 2, 3, 4$.

As a result, suggested SVC algorithms have very low THD compared PWM, also, voltage error of first advanced algorithm is lower than second advanced algorithm. Increase in output voltage causes THD increase, consequently, but it can be acceptable.

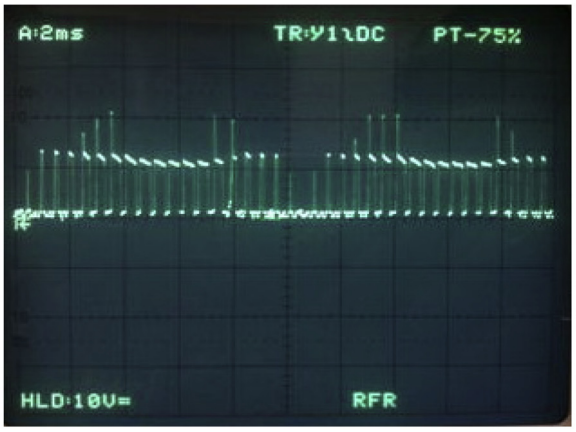
4.2. Experimental results

Cascaded H-bridge 5-level Z-source inverter was built using IRFP460 MOSFETS as the switching devices and MUR820G as fast diodes. A 10V dc voltage source was used to individually supply of each basic units. Z-networks consist of 630 μF capacitors and 2.2 mH inductors. The switching signals that were obtained from PWM algorithm were produced with microcontroller for $B = 1.25$ and $f = 50$ Hz. The switching signals were interfaced to the inverter power switches through optocoupler isolators TLP521. Fig. 13(a) shows photographs of the prototype. It consists of two basic units, two Z-source networks, two DC voltage sources, one full bridge, load $(72 + 11.3j\,\Omega)$ and a microcontroller.

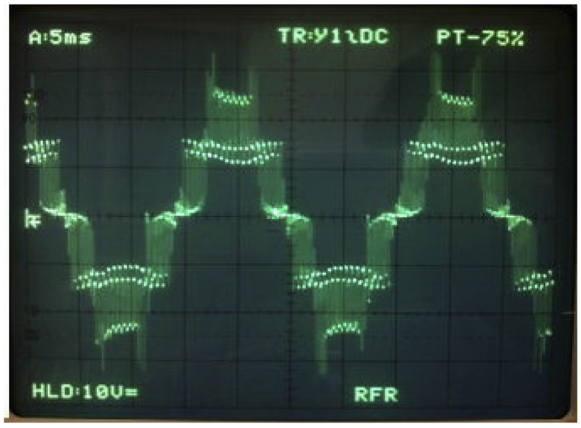
Output voltage of each basic unit is shown in Fig. 13(b), and the levels of v_i are approximately 0, 12.5. As compared to dc voltage source, the amplitude of voltage is boosted according to $B = 1.25$. The load voltage is shown in Fig. 13(c). Measured five levels are approximately 0, ±12.5, ±25. As it can be seen, the results verify the ability of proposed inverter in voltage boosting and generation of desired output voltage waveform.



(a)



(b)



(c)

Figure 13 (a) Photographs of the prototype; (b) output voltage of Z-network (v_i); (c) load voltage (10 V/DIV).

5. Conclusion

This paper employed space vector control as control strategy of cascaded H-bridge multilevel Z-source inverter. Use of Z-source causes more reliability and bucking or boosting capacity of output voltage. In this case, two advanced algorithms proposed make it possible to achieve a wide range of output voltage with lowest THD. These algorithms produce a high-quality voltage with an extremely low switching frequency which can be easily implemented in a standard DSP motor controller. Simulations have verified the proposed algorithms in three levels of output voltages. The simulation results demonstrate the accuracy of suggested algorithms.

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